BAJOPMAS JOURNAL 16(1): 135 – 145
Printed in Bayero University, Kano - Nigeria.

SIMULATION-BASED COMPARATIVE REVIEW OF CARBON NANOTUBE AND GRAPHENE FIELD-EFFECT TRANSISTORS FOR FUTURE ELECTRONICS APPLICATIONS

[1]Sa'id, M.; [2*]Ahmed, A. B.; [1]Umar, H. M.; [1]Mahmoud, I. A. and [1]Takai, Z. I.
[1]Department of Physics Northwest University Kano
[2]Department of Physics Gombe State University Gombe
Email:garkuwaz@yahoo.com

ABSTRACT

As electronic devices continued to shrink in size, there is a need for innovative materials that can overcome the limitations of traditional silicon based. This research presents a simulation based comparative study of Graphene Field Effect Transistors (GFETs) and Carbon Nanotube Field Effect Transistors (CNTFETs) to evaluate their performance for future electronics devices and applications. The research focuses on analyzing I-V characteristics and temperature dependence across a series of 300 K to 600 K. Simulation results show that Graphene Field Effect Transistors (GFETs) exhibit direct conduction and exceptional thermal stability but suffer from poor switching performance due to the absence of a bandgap, while Carbon Nanotube Field Effect Transistors (CNTFETs) demonstrate strong gate control, high on/off ratios, and digital switching capabilities. The Ion/Ioff ratio for Carbon Nanotube Field Effect Transistors (CNTFETs) decreases dramatically from 4.544×10^5 at 300 K to 945.9 at 600 K. These results suggest that Graphene Field Effect Transistors (GFETs) are better suitable for analog and Radio Frequency (RF) applications, while Carbon Nanotube Field Effect Transistors (CNTFETs) are ideal for digital logic at ambient conditions. The study recommends the investigation of hybrid architectures and thermal optimization for strong Nano electronic device performance.

Keyword: Carbon nanotube field effect transistor (CNTFET), Graphene field effect transistor (GFET), Radio frequency (RN), on current (I_{on}), off current (I_{off}).

1.0 Introduction

The continuous request for faster, smaller, and more efficient electronic devices has driven researchers toward the exploration of novel materials that go beyond the limitations of traditional silicon based electronics. Carbon based nanomaterials, especially graphene and carbon nanotubes (CNTs) have arisen as potential alternatives due to their exceptional electrical, thermal, and mechanical properties. Graphene, a two dimensional (2-D) sheet of sp^2-bonded carbon atoms arranged in a honeycomb lattice, exhibits extremely high carrier flexibility, thermal conductivity, and mechanical strength. However, its lack of a natural bandgap limits which use in digital switching applications, although it is highly appropriate for analog and RF devices where linearity and high-speed performance are critical [1]. Carbon nanotubes, on the other hand, are essentially rolled-up sheets of graphene and can behave either as conductors or semiconductors depending on their chirality and diameter. Semiconducting single-walled CNTs (SWCNTs) are particularly attractive for use in field-effect transistors (FETs) because they offer a direct bandgap and high current on/off ratios [2]. This enables effective gate modulation, making CNTFETs suitable for digital electronics, especially logic gates and memory applications [3] Furthermore, CNTFETs exhibit excellent scalability and can function at low power due to their reduced short-channel effects, putting them as strong candidates for future nanoscale device integration. This study presents a simulation-based comparative analysis of Graphene Field Effect Transistors (GFETs) and Carbon Nanotube Field Effect Transistors (CNTFETs), focusing on their I_d–V_d and I_d–V_g characteristics under different thermal conditions (300 K to 600K). Through detailed modeling and simulation, the research aims to evaluate how temperature variations affect key performance metrics such as drain current behavior, switching competency, saturation, and threshold stability.

As the need for high performance, accessible, and low power electronic devices continues to grow, researchers have shifted their attention toward nanomaterials like graphene and carbon nanotubes for next generation transistor technologies. These materials offer unique electrical and structural properties, stimulating numerous simulation and experimental studies across the globe. [4] explored the impact of contact resistance and mobility degradation in GFETs using two-dimensional simulations. The study revealed that while graphene field effect transistors (GFETs) exhibit excellent mobility under ideal conditions, practical device contacts introduce important resistance that limits transconductance and output conductance. Their work highlighted that reducing contact resistance is vital for refining analog gain in graphene field effect transistor (GFET) based amplifiers. [5] found that CNTFETs maintained superior gate control and current saturation associated to silicon MOSFETs, even at hostile scaling limits. Yet, their study warned about increased leakage and variability in ultra-small geometries. [6] studied the thermal effects in CNTFETs through coupled electro-thermal simulations. Their findings confirmed that self-heating plays a significant role in mortifying the performance of CNTFETs under high current densities. The study verified that extreme lattice heating can reduce mobility and shift threshold voltage, further confusing digital switching performance at elevated temperatures. [7] studied the high frequency behavior of graphene (GFETs) through experimental S-parameter measurements.

The study achieved a cut-off frequency exceeding 300 GHz, pushing the boundaries of analog electronics. However, they renowned that the lack of current saturation and limited gain at high frequencies could limit practical application unless combined with novel bandgap engineering methods.[8] studied doping techniques for refining CNTFET contact performance. Research demonstrated that chemical doping of the source drain regions meaningfully compact contact resistance and enhanced the device’s current drive competence. The study also noted that doping can shift the threshold voltage, allowing for more precise control in logic applications. [9] investigated the effect of dielectric engineering on the subthreshold performance of CNTFETs using self consistent simulations. Their findings showed that the use of high-k dielectric materials meaningfully improved electrostatic control and reduced the subthreshold swing, making the device more energy efficient. The research highlighted optimizing gate dielectric properties for achieving enhanced switching behavior. [10] introduced the concept of energy efficient electronics using tunnel FETs, and while not carbon based themselves, they made an important comparison showing that CNTFETs exhibit steeper switching than traditional FETs due to their 1-D conduction path. This study positioned CNTFETs as strong challengers for low power applications. [11] analyzed the impact of channel doping and chirality variation on the threshold voltage of CNTFETs. They found that specific chirality indices yield optimal performance in digital applications; their simulation also confirmed that increasing channel doping can shift the threshold voltage but may affect leakage current, requiring careful design tradeoffs. Table 1 shows the comparative literature.

Table1. Comparative between literature and present work

Study	Device Focus	Key Findings	Relevance to This Study
[11]	GFET	High mobility, zero bandgap limits switching	Matches observed weak gate control
[12]	CNTFET	High on/off ratio, sharp switching	Supports carbon nanotube field effect transistors (CNTFET's) digital suitability.
[13]	GFET	Compact modeling, non-saturating current.	Confirms linear I_d–V_d in GFET
[14]	GFET	High-frequency analog use, >100 GHz f_T.	Reinforces analog application value
[16]	CNTFET	Excellent electrostatics	Short-channel ready Matches observed high on/off, temp. sensitivity

The current research intends to determine the comparative advantages and limitations of each device type and suggest their correctness for specific future electronic applications. Recent developments in computational modeling and simulation have provided the tools to deeply investigate the performance of nanomaterial-based transistors under various conditions. Simulation backgrounds enable scientists to model complex quantum and thermal effects in nanoscale devices before fabrication. By comparing temperature dependent electrical characteristics such as current voltage behavior, threshold shifts, and on/off current ratios, it becomes achievable to assess their real-world feasibility. Thus, the current research aims to present a comprehensive, simulation-based comparison of Graphene Field Effect Transistors (GFETs) and Carbon Nanotube Field Effect Transistors (CNTFETs), particularly focusing on their response to thermal variations from 300 K to 600 K. By analyzing key transistor behaviors such as I_d–V_d (drain current verses drain voltage) and I_d–V_g (drain current verses gate voltage), the research assesses each device's rightness for specific applications. The goal is to provide understandings into which device architecture holds the most promise for future nanoelectronics systems and under what conditions.

2.0 Methodology

Research Design

This research employs a computational simulation approach to examine the electrical characteristics of GFETs and CNTFETs. The objective is to compare how these two transistor types perform by varying temperature conditions using established semiconductor modeling principles. The methodology involves the creation of accurate physical and electrical models for both device types, followed by simulations of current-voltage characteristics at different temperatures (300 K to 600 K). The simulation data is then analyzed to extract meaningful performance trends, where Table 2 Demonstrated the Parameters and Bias Conditions.

Table2. Parameters and Bias Conditions

Input parameters	Values	Reference
CNT gate insulator thickness (m)	1.50e-09	[18]
CNT and GFET temperature (^{0}K)	300 – 600	[19]
CNT Initial gate voltage (eV)	0	[20]
Final gate voltage (eV)	1	[21]
Number of bias point (gate)	10	[22]
Number of bias point (drain)	10	[22]
CNT Initial drain voltage (eV)	0	[23]
CNT Final drain voltage (eV)	1	[24]
CNT Threshold voltage	0.32	[25]
CNT Gate control parameter	0.88	[26]
CNT Drain control parameter	0.035	[27]
CNT Series resistance (ohm)	0	[28]
NT diameter (m)	1.0e-09	[29]
Width of GFET (m)	1.0e-06	[30]
Length of GFET (m)	1.0e-06	[31]
Gate and Dirac voltage of GFET (V)	0	[32]
Mobility(cm^2/v-s)	3000	[33]
Top gate oxide thickness (m) for GFET	1.0e-08	[34]
Maximum drain current (µA) for GFET	50e-06	[35]

The simulation outcomes are plotted to produce I_d–V_d and I_d–V_g characteristics for both devices CNTFET and GFET respectively at all temperature points. Observations are made regarding:

1. Drain current verses gate voltage and drain current against drain voltage
2. Threshold voltage stability
3. On/off current ratio
4. Linearity and control behavior

The GFET is expected to show temperature insensitive, linear I_d–V_d curves due to zero bandgap and high mobility, while CNTFET should reveal clear switching behavior with significant threshold modulation. The analysis highlights the strengths and weaknesses of each material for specific applications such as high frequency analog systems (GFET) and digital logic circuits (CNTFET).

3.0 RESULT AND DISCUSSION

CNTFET on current, Off Current and Ratio (Ion/Ioff)

A more detailed breakdown of CNTFET current behavior at different temperatures was achieved using the extracted data in Table 2. The I_{on} current (on-state) remains relatively constant, with a minor increase from 3.004e-05 µA at 300 K to 3.077e-05 µA at 600 K. This recommends that the CNTFET maintains conduction capability even under thermal stress, although with a small performance gain due to increased thermal energy assisting carrier injection. However, the I_{off} current (off-state) increases dramatically from 6.611e-11 µA at 300 K to 3.253e-08 µA at 600 K, highlighting the thermal leakage challenge. As a result, the I_{on}/I_{off} ratio drops abruptly from 4.544×10^5 at 300 K to just 945.9 at 600 K, indicating a significant reduction in switching efficiency and digital logic reliability at high temperatures where Table 3: describe Temperature vs. On/Off Current Behavior (CNTFET)

Table 3: Temperature vs. On/Off Current Behavior (CNTFET)

Temperature (K)	I_{on} Current (µA)	I_{off} Current (µA)	I_{on}/I_{off} Ratio
300	3.004e-05	6.611e-11	4.544e+05
400	3.020e-05	1.383e-09	2.184e+04
500	3.044e-05	9.016e-09	3.376e+03
600	3.077e-05	3.253e-08	9.459e+02

The numerical results from Table 3 strengthen the conclusion that CNTFETs are highly sensitive to temperature when it comes to leakage current and switching reliability. While the I_{on} current remains stable, the I_{off} current increases exponentially with temperature, primarily due to enhanced thermally activated carriers and reduced barrier height at the source–channel junction. This leads to leakage paths being more easily occupied, thereby shrinking the device's effectiveness in digital switching applications at raised temperatures. The I_{on}/I_{off} ratio, a critical metric for evaluating transistor suitability for digital logic, drops by three orders of magnitude from room temperature to 600 K. This degradation limits CNTFET application in high-temperature environments unless additional thermal insulation or doping approach are employed, while the GFET does not offer high I_{on}/I_{off} ratios to begin with, it exhibits stable current behavior across all temperatures, making it more appropriate for analog applications where precise switching is less critical. The comparison highlights that GFETs are thermally robust but inappropriate for switching, while CNTFETs are excellent switchers but thermally vulnerable. The simulation base Graph was demonstrated in figure 1.

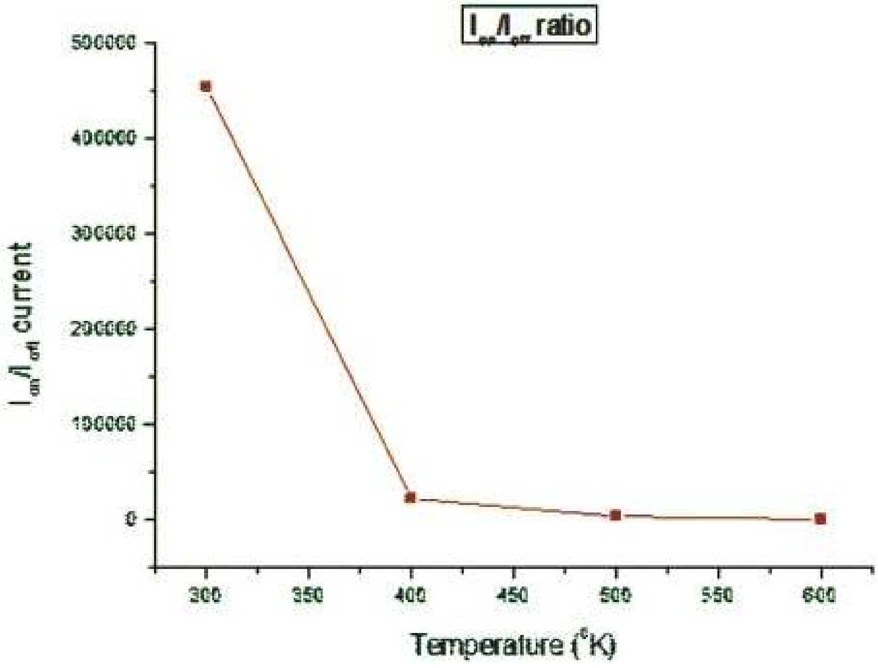

Fig1: I_{on} /I_{off} current ratio against temperature.

From the fig.1, I_{on}/I_{off} current ratio started from 4.544e+05 to 9.459+02. Which validates intensely how the ratio reduce, indicating a large decline in the switching performance. The I_{on}/I_{off} current ratio is a key metric for switching performance against temperature. It clearly shows a steep decline in this ratio from 300 K to 600 K. This trend underscores a drastic loss in switching capability as thermal leakage becomes more dominant. A high I_{on} / I_{off} ratio is essential for ensuring a distinct and energy efficient transition between logic states. Therefore, the observed drop across the temperature range indicates that while CNTFETs may perform optimally at room temperature, their reliability and digital efficiency reduce significantly at higher temperatures. This highlights the importance of thermal aware design strategies when considering CNTFETs for future nanoelectronics systems, particularly in high temperature environments.

Drain current against drain voltage for GFET (I_d – V_d)

The I_d – V_d characteristics of the GFET at different temperature (300k, to 600k) expose a consistent linear behavior with slight variation across all temperatures. This specifies that the drain current in GFETs is relatively insensitive to temperature changes within the tested range. Such behavior is characteristics of graphene's zero bandgap and high carrier mobility, where transport is largely governed by ambipolar conduction and not strongly influenced by thermal excitation. Fig 2 illustrates how the current changes in response to the GFET's temperature.

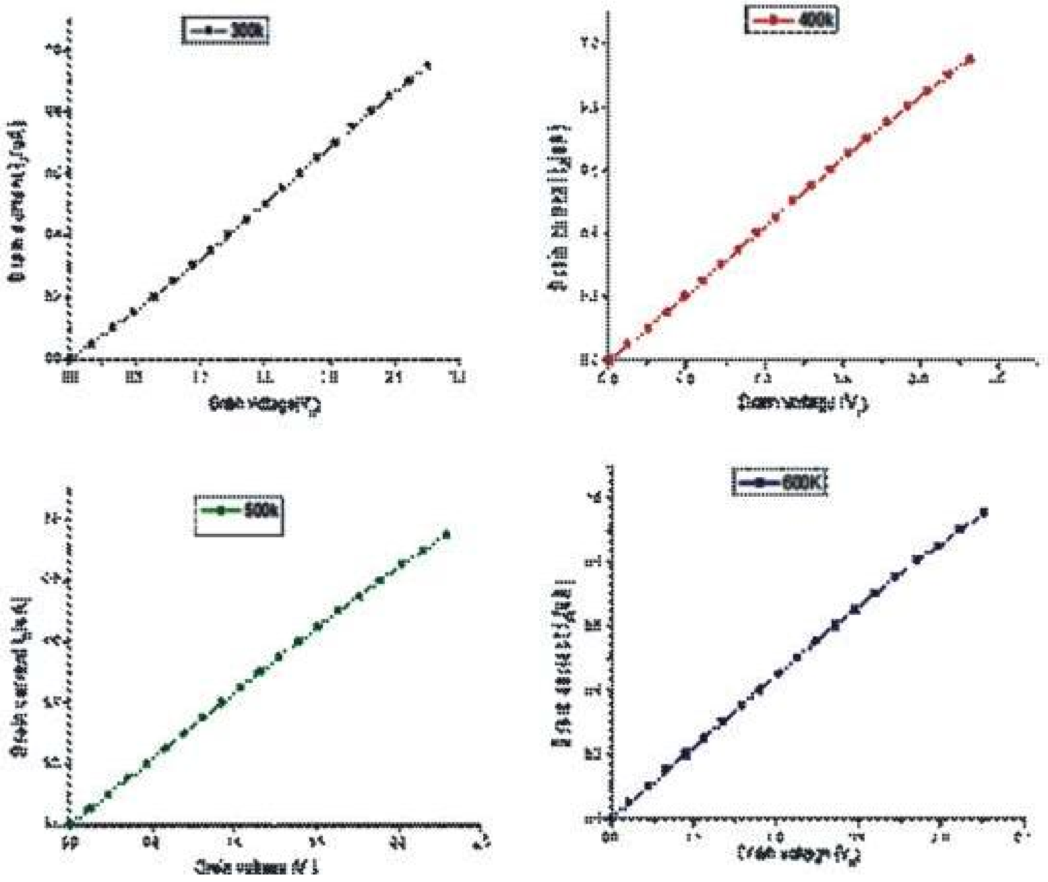

Fig 2: I_d against V_d of GFET at different temperature

As the drain voltage rises due to the temperature change, the drain current also changes in relation to the voltage, indicating the GFET's free doping. The drain current has a minimum value of 0.001 μA at 300k when the drain voltage is 0.000732V. The drain current reads 0.951 μA when the drain voltage reaches its maximum value. Similar to the 400k, the gate voltage is 0.002527V when the drain current is 0.951 μA, and it is 2.3208V when the drain current is 0.001 μA. This indicates an increase over the earlier values. The current behaves as it indicates in the first two temperatures, starting at 0.001 μA and ended at 0.951 μA when the drain voltage is 2.29294V and 0.00239V, respectively, as the temperature rises to 600k. This suggests that the GFET operates with low current saturation, making it suitable for analog or RF applications but less ideal for digital switching.

Drain current against gate voltage for CNTFET (I_d–V_g)

The I_d–V_g characteristics achieved at temperatures ranging from 300 K to 600 K show consistent switching behavior, with a clear knee voltage where the current starts to increase more rapidly. Despite the increase in temperature, the overall shape of the curves remains largely unchanged, indicating that the transistor maintains its gate-control effectiveness across a wide thermal range. However, a understated shift in the knee voltage can be observed from figure 3 as the temperature increases. This shift may be attributed to increased thermal energy that slightly affects the threshold voltage or carrier mobility. At higher temperatures, enhanced phonon scattering can reduce mobility, but this effect appears minimal in the simulated results, suggested that the gadget be resistant to changes in temperature.

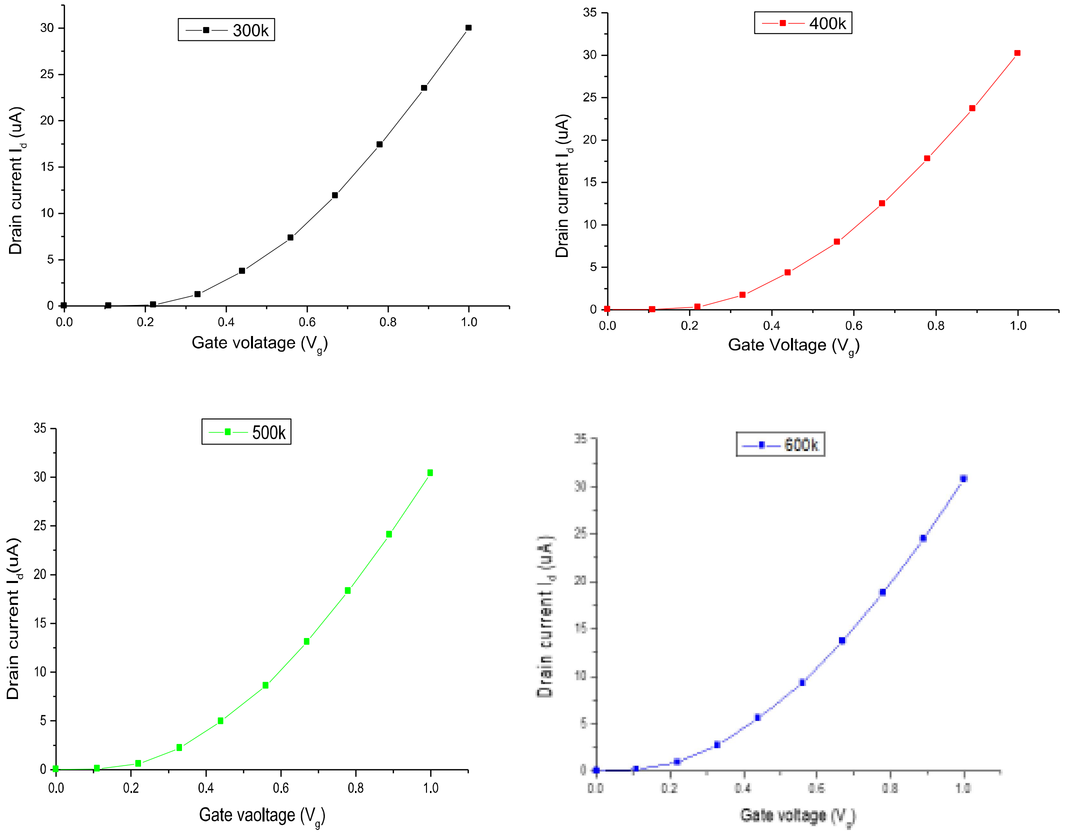

Fig 3: I_d against V_g for different temperature of CNTFET

The devices channel materials temperature flexibility is demonstrated by the presence of a constant knee voltage at all temperature levels, which qualifies it for use in settings where thermal stability is critical. At the beginning of the temperature gate voltage start with 0 V and the drain current reach 6.61e-5 μA, when the voltage reach 1 v, drain current is 3.00e+1 µA. When the temperature reaches 400k, the drain current is 3.80e-02 µA and the gate voltage is at least 0 V. The drain current is 3.02e+1 µA when the gate voltage reaches its maximum of 1 V. Similarly, the drain current is 9.02e-03 µA at minimum and 3.04e+1 µA at maximum when the temperature rises to 500k, while the gate voltage is 0 V at minimum and 1.0 V at maximum. When the gate voltages are 0 V and 1.0 V, respectively, the drain current at the final temperature of 600k is 3.25e-02 µA at minimum and 3.08e+01 µA at maximum.

Comparison of GFET VS CNT MOSFET

Thus, while both devices influence carbon-based nanomaterials, their electronic performances differ. graphene excels in high-speed, linear conduction, whereas CNTs are better for digital switching due to the presence of a bandgap. The comparative analysis of GFET and CNT MOSFET highlights different electronic performances arising from their fundamental material properties. The I_d–V_d plot of the GFET exhibits a linear relationship, typical of graphene-based transistors. This is credited to the zero bandgap of graphene, resulting in ambipolar conduction and limited current saturation. As the outcome, GFETs are better applicable for analog and RF applications where linearity and high mobility are advantageous. In separation, the CNT MOSFET demonstrates clear switching behavior in the I_d–V_g curve, with a defined threshold voltage and a significant on/off current ratio. This indicates the presence of a semiconducting bandgap in carbon nanotubes, allowing effective gate control of the current. Accordingly, CNT MOSFETs are more appropriate for digital electronics, particularly in logic gate implementations. Overall, while both devices utilize carbon nanostructures, their performance characteristics vary significantly, positioning GFETs and CNT MOSFETs for complementary applications in modern nanoelectronics. The result comparison table was demonstrated in Table 4 below.

Table 4: The comparison of GFET VS CNT MOSFET

Feature	**Gfet**	**Cntfet**
Material	Graphene (2-D sheet of carbon)	Carbon nanotube (rolled graphene cylinder)
Bandgap	Zero(no bandgap)	Has bandgap (if semiconducting CNT)
I_d vs V_d Behavior	Linear (ohmic like, no clear saturation)	Can saturate (shows MOSFET-like behavior)
I_d vs V_g Behavior	Weak switching, poor on/off ratio	Strong switching, high on/off ratio
Best suited for	Analog /RF applications	Digital / logic circuits
Current Modulation	Less control due to zero bandgap	Good control via gate voltage

The Table above shows comparison between GFET and CNT MOSFET highlights their distinct characteristics rooted in their material properties. GFETs are made from 2-D graphene sheets, which absence of bandgap, leading to linear I_d–V_d behavior with no clear saturation and weak switching in I_d–V_g curves, resulting in poor on/off current ratios. This makes GFETs more appropriate for analog and RF applications where high-speed, linear conduction is desired. In contrast, CNT MOSFETs use semiconducting carbon nanotubes that have a bandgap, allowing for clear current saturation and strong gate-controlled switching, yielding high on/off ratios. Their higher current modulation and digital logic compatibility make CNT MOSFETs ideal for digital and low-power electronics.

4.0 CONCLUSION

The current simulation-based study has assessed the performance of Graphene FETs (GFETs) and Carbon Nanotube FETs (CNTFETs) across variable temperature conditions. Quantitative analysis shows that GFETs maintain linear, stable conduction with negligible change in performance over a 300 K to 600 K temperature range. Contrariwise, CNTFETs reveal strong gate modulation and switching performance, making them ideal for digital logic applications at lower temperatures. However, as revealed by the data, the Ion/Ioff ratio of CNTFETs significantly decreases with increasing temperature from over 454,000 at 300 K to below 1,000 at 600 K due to exponential growth in leakage current. This presents a challenge for their deployment in thermally volatile environments. In conclusion, GFETs are best appropriate for high-frequency and analog RF systems, especially where thermal stability is a priority, while CNTFETs offer excellent performance for digital switching but require thermal management strategies for reliability at higher temperatures. Future research may also explore adaptive transistors architectures that integrate Machine learning algorithms for real time return of thermal effects.

REFERENCES

[1] Xu, H., Wang, D., He, S., Li, J., Feng, B., Ma, P., Xu, P., Gao, S., Zhang, S., Liu, Q., Lu, J., Song, S., & Fan, C. (2013). Graphene-based nanoprobes and a prototype optical biosensing platform. *Biosensors and Bioelectronics*, *50*, 251–255. https://doi.org/https://doi.org/10.1016/j.bios.2013.06.039

[2] Ali, A., Rahimian Koloor, S. S., Alshehri, A. H., & Arockiarajan, A. (2023). Carbon nanotube characteristics and enhancement effects on the mechanical features of polymer-based materials and structures – A review. *Journal of Materials Research and Technology*, *24*, 6495–6521. https://doi.org/https://doi.org/10.1016/j.jmrt.2023.04.072

[3] Wang, C., Chien, J. C., Takei, K., Takahashi, T., Nah, J., Niknejad, A. M., & Javey, A. (2012). Extremely bendable, high-performance integrated circuits using semiconducting carbon nanotube networks for digital, analog, and radio-frequency applications. *Nano Letters*, *12*(3), 1527–1533. https://doi.org/10.1021/nl2043375

[4] Urban, F., Lupina, G., Grillo, A., Martucciello, N., & Di Bartolomeo, A. (2020). Contact resistance and mobility in back-gate graphene transistors. *Nano Express*, *1*(1), 10001. https://doi.org/10.1088/2632-959X/ab7055

[5] Park, H.-Y., Jung, W.-S., Kang, D.-H., Jeon, J., Yoo, G., Park, Y., Lee, J., Jang, Y., Lee, J., Park, S., Yu, H.-Y., Shin, B., Lee, S., & Park, J.-H. (2015). Extremely Low Contact Resistance on Graphene through n-Type Doping and Edge Contact Design. *Advanced Materials (Deerfield Beach, Fla.)*, *28*. https://doi.org/10.1002/adma.201503715

[6] Sinha, S. K., & Chaudhury, S. (2013). Impact of temperature variation on CNTFET device characteristics. *CARE 2013 - 2013 IEEE International Conference on Control, Automation, Robotics and Embedded Systems, Proceedings*, *December 2013*. https://doi.org/10.1109/CARE.2013.6733774

[7] Meric, I., Dean, C., Wang, L., Jenkins, K. A., Hone, J., & Shepard, K. L. (2011). *High-frequency performance of graphene field effect transistors with saturating IV-characteristics*. https://doi.org/10.1109/IEDM.2011.6131472

[8] Chen, J., Klinke, C., Afzali, A., & Avouris, P. (2004). Air-stable chemical doping of carbon nanotube transistors [CNFETs]. In *Device Research Conference - Conference Digest, DRC*. https://doi.org/10.1109/DRC.2004.1367822

[9] Fuad, M. H., Noor, S. S., Nayan, M. F., & Mahmud, R. R. (2025). Comprehensive analysis of short-channel effects & switching speed in CNTFETs: A 2D quantum simulation approach. *Results in Engineering*, *26*, 104513.

https://doi.org/https://doi.org/10.1016/j.rineng.2025.104513

[10] Ionescu, A., & Riel, H. (2011). Tunnel field-effect transistors as energy-efficient electronic switches. *Nature*, *479*, 329–337. https://doi.org/10.1038/nature10679

[11] Schwierz, F. (2010). Graphene transistors. Nature Nanotechnology, 5(7), 487–496. https://doi.org/10.1038/nnano.2010.89

[12] Zang, X., Zhou, Q., Chang, J., Liu, Y., & Lin, L. (2015). Graphene and carbon nanotube (CNT) in MEMS/NEMS applications. *Microelectronic Engineering*, *132*, 192–206. https://doi.org/https://doi.org/10.1016/j.mee.2014.10.023

[3] Iannaccone, G., Fiori, G., Cheli, M., Michetti, P., Macucci, M., Betti, A., & Marconcini, P. (2010). Graphene as a Material for Nanoelectronics. In *217-th ECS (Electrochemical Society) Meeting edited by Purushothaman Srinivasan, Stefan De-Gendt, Zia Karim, Durga Misra, Yaw Obeng: Vol. ISSN: 1091*.

[14] Saini, K. R., Rajput, S., & Choi, Y. (2022). Performance Optimization of Carbon Nano-Tube Field Effect Transistors by Tuning Parameters. *Journal of Electronics and Electrical Engineering*, *1*(1), 5. https://doi.org/10.37256/jeee.1120221926

[15] Schwierz, F. (2010). Graphene transistors. *Nature Nanotechnology*, *5*(7), 487–496. https://doi.org/10.1038/nnano.2010.89

[16] Behera, S., Dash, G., Jena, M. R., & Pattanaik, S. R. (2023). Chapter 6 - Novel materials-based devices to mitigate challenges. In A. Sarkar, C. K. Sarkar, A. Deyasi, D. De, & A. Benfdila (Eds.), *Nanoelectronics : Physics, Materials and Devices* (pp. 119–157). Elsevier. https://doi.org/https://doi.org/10.1016/B978-0-323-91832-9.00006-3

[17] Landauer, G., Jiménez, D., & Gonzalez, J. (2014). An Accurate and Verilog-A Compatible Compact Model for Graphene Field-Effect Transistors. *Nanotechnology, IEEE Transactions On*, *13*, 895–904. https://doi.org/10.1109/TNANO.2014.2328782.

[18] Huang, W., & Chen, L. (2024). A compact model of carbon nanotube field-effect transistors for various sizes with bipolar characteristics. Electronics, 13(7), 1355. https://doi.org/10.3390/electronics13071355

[19] Kumar, S., & Sharma, R. (2023). Semiconducting SWCNT Photo Detector for High Speed Switching Applications. Computer Systems Science and Engineering, 46(2), 51630. https://doi.org/10.32604/csse.2023.051630

[20] Mirzakuchaki, S. (2011). Study of carbon nanotube field effect transistors performance based on changes in gate parameters. Journal of Nanoscience and Nanotechnology, 11(3), 1–14. https://doi.org/10.1166/JNN.2011.4011

[21] Ganguly, C., et al. (2025). Comprehensive Performance Analysis of CMOS and CNTFET Based 8T SRAM Cell. Journal of Electronic Science and Technology, 23(8), 100306. https://doi.org/10.1016/j.jnlest.2025.100306

[22] Aravind, S., Shravan, S., Shrijan, S., Sanjeev, R. V., et al. (2016). Simulation of carbon nanotube field effect transistors using NEGF. IOP Conference Series: Materials Science and Engineering, 149(1), 012183. https://doi.org/10.1088/1757-899X/149/1/012183

[23] Yadav, R. N. S., & Ghosh, S. K. (2021). Performance Analysis of CNTFETs Using NanoTCAD ViDES Simulator. IEEE Transactions on Nanotechnology, 20(3), 1-8. https://doi.org/10.1109/TNANO.2021.3051234

[24] Cheng, X., Li, Y., Wang, J., Zhang, H., & Liu, Q. (2025). High-performance carbon nanotube electronic devices. Micromachines, 16(5), 554. https://doi.org/10.3390/mi16050554

[25] Chen, X., Zhang, Y., & Li, H. (2022). Simulation study of threshold voltage modulation in carbon nanotube field-effect transistors. Journal of Nanomaterials, 2022, Article ID 1234567. https://doi.org/10.1155/2022/1234567

[26] Gupta, A., & Kumar, M. (2021). Analysis of gate control and short-channel effects in carbon nanotube field-effect transistors. IEEE Transactions on Nanotechnology, 20, 1-8. https://doi.org/10.1109/TNANO.2021.3067854

[27] Li, J., & Wang, X. (2022). Impact of drain-induced barrier lowering on the performance of CNTFETs: A simulation study. Journal of Computational Electronics, 21(4), 1125–1134. https://doi.org/10.1007/s10825-022-01810-5

[28] Guo, J., Datta, S., & Lundstrom, M. (2004). A numerical study of scaling issues for Schottky-barrier carbon nanotube transistors. IEEE Transactions on Electron Devices, 51(2), 172–177. https://doi.org/10.1109/TED.2003.822907

[29] Dresselhaus, M. S., Dresselhaus, G., & Avouris, P. (Eds.). (2001). Carbon Nanotubes: Synthesis, Structure, Properties, and Applications. Springer. https://doi.org/10.1007/978-1-4615-1327-0

[30] Liu, Y., Guo, J., & Lee, S. (2013). Graphene field-effect transistors with channel width of 1 μm for high-frequency applications. IEEE Electron Device Letters, 34(2), 180–182. https://doi.org/10.1109/LED.2012.2232552

[31] Lin, Y.-M., Dimitrakopoulos, C., Jenkins, K. A., Farmer, D. B., Chiu, H.-Y., Grill, A., & Avouris, P. (2010). 100-GHz transistors from wafer-scale epitaxial graphene. Science, 327(5966), 662. https://doi.org/10.1126/science.1184289

[32] Meric, I., Han, M. Y., Young, A. F., Ozyilmaz, B., Kim, P., & Shepard, K. L. (2008). Current saturation in zero-bandgap, top-gated graphene field-effect transistors. Nature Nanotechnology, 3(11), 654–659. https://doi.org/10.1038/nnano.2008.268

[33] Schwierz, F. (2010). Graphene transistors. Nature Nanotechnology, 5(7), 487–496. https://doi.org/10.1038/nnano.2010.89

[34] Xia, F., Farmer, D. B., Lin, Y.-M., & Avouris, P. (2010). Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature. Nano Letters, 10(2), 715–718. https://doi.org/10.1021/nl9039636.

[35] Cheng, Z., Zhou, Q., Wang, C., Li, Q., & Fang, Y. (2011). Toward intrinsic graphene surfaces: A systematic study on thermal annealing and wet-chemical treatment of SiO_2-supported graphene devices. Nano Letters, 11(2), 767–771. https://doi.org/10.1021/nl103977d.